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Modelling of Tri Gate FinFETs

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Abstract : Tri-gate FinFET's are the promising replacements for the double gate structures. The Schotkky barrier structure is one of the tri-gate FinFETs, it has good control on I-ON but the expected OFF current is not achieved.To overcome this fin problems two structures namely Raised Source Drain &DSS are modeled and 2-D simulation are performed on them which resulted in increased to Silicide flare out. The metal bars that are strapped on the Fins individually on RSD&DSS structures resulted in lower silicide flareout for lower Fin pitches but resulted in delay for higher Fin pitches.A new structure called recessed strap FinFET is modeled using vias to over come this problem and the results are studied using Sentarus TCAD from Synopsys.
Key words: Capacitance, dopant segregation, FinFET, metallic source/drain (MSD), raised source/drain (RSD), Schottky barrier (SB).

Introduction

In recent years, there has been a growing interest in metallic source/drain (MSD) technology as a replacement for conventional doped source/drain technology, particularly for thin-body MOSFETs which have relatively large parasitic source/drain resistance. Over time, it has become clear that optimal MSD MOSFET performance is achieved by using heavily doped source/drain extensions (SDEs) adjacent to the Schottky barrier (SB) contacts, typically formed by dopant pileup or implant to silicide (ITS). The resulting structures have been called dopant-segregated Schottky (DSS) or modified SB MOSFETs[1-6].

The claimed benefits for MSD technology (either as conventional SB or "enhanced" DSS MOSFETs) have included improved short channel effect (SCE) immunity due to the source-side SB and the abrupt silicide-to-silicon junction, as well as carrier-injection velocity enhancement due to SB injection at the source. However, largely dispelled these claims and instead showed that optimized DSS MOSFETs offer no fundamental improvement in ON-state current I_{ON} when compared to optimized raised source/drain (RSD) MOSFETs.The main conclusion of was that the decision to move toward DSS MOSFETs or RSD MOSFETs in future technology nodes would depend on factors other than I_{ON}, such as ease of process integration or some other metric/s[1-6].

Simulation methodology and extraction[1-6]

Simulation Methodology

Sentaurus TCAD simulator from Synopsys is used to perform all the simulations. This simulator has many modules and the following are used in this study.

- Sentaurus structure editor (SDE): To create the device structure, to define doping, to define contacts, and to generate mesh for device simulation
- Sentaurus device simulator (SDEVICE): To perform all DC, AC and noise simulations
- Inspect and Tecplot: To view the results.

Approach

2-D Device Structure

This paper begins with a 2-D double-gate (DG) DSS NMOS structure, as shown in Fig. 1. L_G = 10 nm, $t_{body} = L_{sp} = L_{SDE}$ = 7 nm, V_{DD} = 1 V, I_{OFF} = 100 nA/μm, and t_{ox} =1 nm. The SDE doping profile is Gaussian with peak concentration N_{SDE} at the source/drain SB junctions; L_{SDE} is the distance from the SB junctions to where the SDE concentration drops to 1×10^{18} cm $^{-3}$ (the cutoff between degenerate and nondegenerate doping). L_{sp} is the gate underlap to the source/drain SB junctions (also the sidewall spacer thickness if one neglects lateral silicidation, as done here), where the sidewall spacer is made of silicon nitride[13], t_{flare} is the amount by which the source/drain silicide regions adjacent to the sidewall spacer flare out from the fin structure, and all other terms have their usual meaning. The metal gate height t_{gate} = 20 nm, the body doping is 1×10^{15} cm^{-3} p-type, and N_{SDE} = 3×10^{20} cm^{-3}. The SB height (SBH) at the *M*–*S* interface is set to 0.1 eV in all the cases simulated here (including the 3-D structures shown later), which is reasonable considering the reported data on dopant segregation and interface passivation by Group-VI species, as well as the modeling results. The work function of the silicide φ_M is varied independently from that of the SB contacts. Although full 3-D modeling is necessary to capture all physical effects taking place in FinFETs, particularly when simulating process splits, the purpose of considering the 2-D structure here is to clearly illustrate the effect of silicide gating to the reader before investigating its effect in the more complex environment of a full 3-D structure later in this paper.

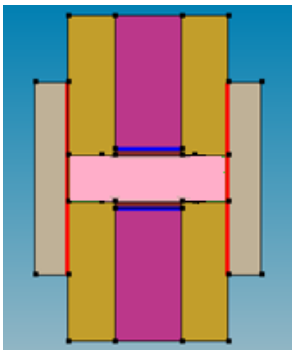


Fig.1 2-D DG DSS structure

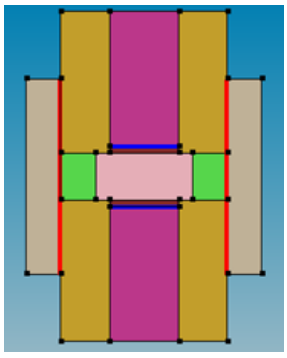


Fig.2 2-D DG DSS with doping at corners

Modeling Setup and Assumptions

Since this paper focuses on HP FinFETs, gate leakage and band-to-band tunneling leakage are ignored. Moreover, the silicide and metal/via (for 3-D modeling, shown later) resistances are assumed to be negligible, as they are much lower than that of the heavily doped silicon source/drain regions. Quantization effects are also excluded in this paper to simplify the modeling approach, particularly for the 3-D structures. (Although not shown here, the effect of silicide gating is about the same, if quantization is included.) Since t_{body} = 7 nm here, the effect of quantization on the SBH is small anyway. For example, if one overestimates this effect by assuming an infinite square well formed by the silicon and surrounding dielectrics, the SBH increase due to quantization (in electronvolts) is $0.376/(m^* t_{body})$, where $m^*$is the effective mass in the quantization direction (0.92 in this case) and t_{body} is expressed in units of nanometers. As a result, the worst case SBH increase is 58 mV for t_{body} = 7 nm. Considering that N_{SDE} here is set to 3×10^{20} cm^{-3} and given the results in[5] for low SBH and high N_{SDE}, this slight SBH increase will not affect I_{ON} significantly. Any effect of quantization is therefore primarily a threshold voltage shift and a reduction in mobility, neither of which would alter the results of a comparative study between DSS and RSD FinFETs.

Effect of silicide gating on DSS Finfet performance

Fig. 2 shows the effect of t_{flare}on I_{ON} for NiSi and also for a conduction band-edge silicide (with φ_M = 4.07 eV). For t_{flare} = 0 nm, both silicides exhibit the same I_{ON}, which degrades as t_{flare} increases. This is due to the fringing field effect of the silicide-depleting carriers from the heavily doped SDE region If L_{sp} is increased to offset lateral silicidation, then forming abrupt heavily doped SDE regions becomes more difficult, regardless of whether dopant pileup or ITS is utilized. For dopant pileup, N_{SDE} drops as the silicidation front progresses. Thus, increasing L_{sp} will mean that the silicidation process must progress further laterally for the same L_{SDE} and contactto-gate edge spacing, thereby reducing N_{SDE} and increasing contact resistance R_c.

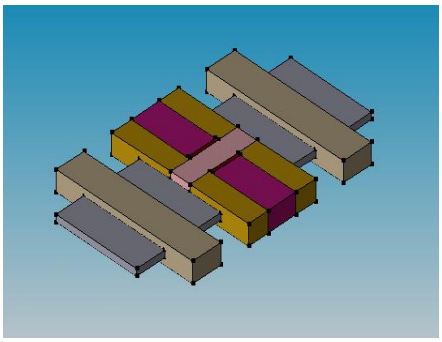


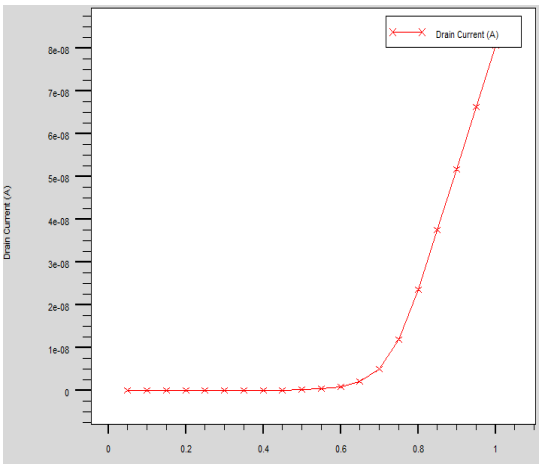
Fig. 3. Three-dimensional illustration of the DSS FinFET with silicides

However, this lateral silicidation encases some silicide between the top and bottom sidewall spacers, resulting in zero localized t_{flare} and, therefore, zero silicide gating effect from the silicide region closest to the SDE region. If ITS is utilized instead of dopant pileup, the portion of the silicide overlapped by the sidewall spacer ends up not being exposed to the SDE implant, resulting in a difference in silicide grain size in the implanted region (smaller grains due to implant damage) and the spacer-protected region (larger grains). It has been shown[28] that this grain size affects the diffusion and amount of barrier lowering achieved with low work function metals in NiSi, with some evidence also for phosphorus in NiSi.

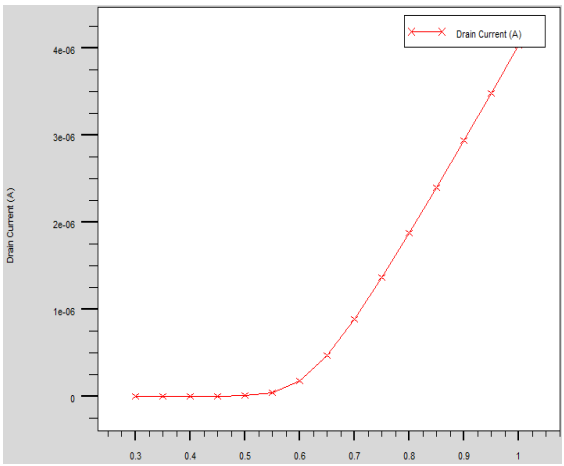
Results and Discussion

Gate Voltage versus drain current:

The graphs shown below are between input gate voltage and drain current with and without the silides.



Gate volage(V)
Figure.4: I-D curve for DSS structure

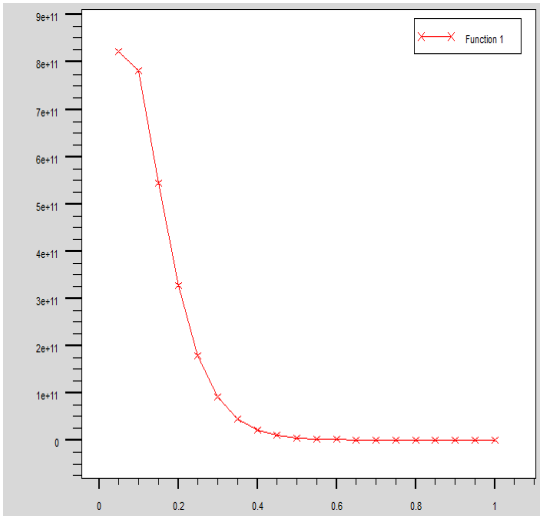


Gate volage(V)
Figure.5: I-D curve for DSS silicide structure

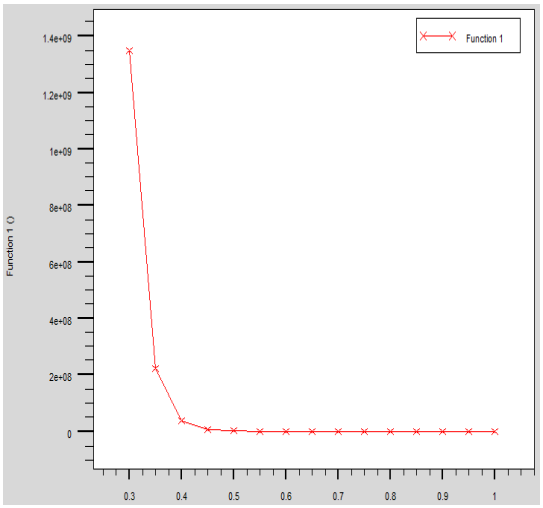
The I-D current should increase linearly beyond the threshold voltage of the device with respect to the input gate voltage.these corner effects can be reduced by doping heavily at the corners of the channel.

Gate voltage versus resistance:

The graphs below are between input gate voltage and resistance with and without the silicides DSS .



Gate volage(V)
Figure.6: resistance curve for DSS structure

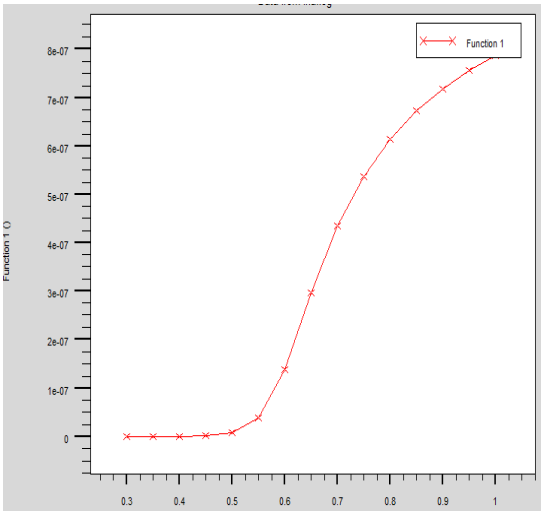


Gate volage(V)
Figure.7: resistance curve with DSS silicides

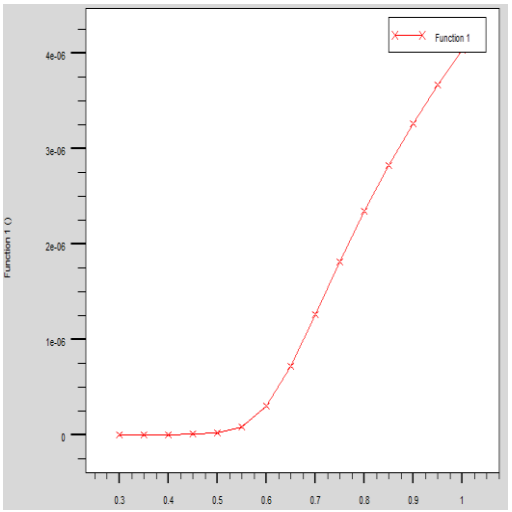
The resistance value of the device should decrease linearly and becomes zero when the gate voltage had reached the threshold voltage value.Here in the below graph, the peak value of the resistance i.e the resistance of the device without corner effects is greatly reduced when compared to the resistance with corner effects.

Gate voltage versus transconductance:

The graphs shows relation between input gate voltage and transconductance with and without the silicides.



Gate volage(V)
Figure.8: transconductance curve for DSS



Gate volage(V)
Figure.9: transconductance curve for DSS silicides

The transconductance value of the device should increase linearly beyond the threshold value and reached its maximum value. For a good FinFET device the transconductance value should be more. Thus, comparing the graphs of the transconductance without and with silicides, the transconductance value is greatly increased.

Table I. Typical Device Dimensions

Parameters	Nominal Value
Gate Length	10 nm
Fin Width	7 nm
Source width	5 nm
Source length	27 nm
Gate oxide thickness	1 nm
Underlap	7 nm
Channel depth	12nm

Table II. Device With Silicides

Parameters	Range
Gate Length (L_{g1} and L_{g2})	10 nm
Channel depth (Ld)	12nm
Fin Width ($W_{fin1}$and W_{fin2})	7 nm
Source width (SW_1 and SW_2)	5 nm
Source length (SL_1 and SL_2)	27 nm
Gate oxide thickness (T_{ox1} and T_{ox2})	1 nm
Silicides length	30nm
Fin pitch	50nm
Underlap (L_{un1} and L_{un2})	7 nm

Table III. Constraints For Silicides

Gate Work Function	4.85
Constant doping value	1e18
Analytical doping value(Nsde)	3e20

Conclusion

A 2-D and 3-D TCAD study was performed to investigate the optimum source/drain and contact designs for aggressively scaled FinFETs. It was found that silicide gating, which is a fringing field effect that originates from the silicide contacts, negatively affects both DSS and RSD FinFET performances. As a result, silicide gating strongly influences the optimum source/drain design for both DSS and RSD FinFETs, to the point where neither structure achieves a universal performance advantage over all ranges of FP and fin height when 3-D parasitics are accounted for. Therefore, a new FinFET source/drain architecture has been proposed, called the RS DSS FinFET, which combines the merits of both DSS and RSD FinFETs to achieve equivalent or improved performance over all ranges of FP and Fin height.

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